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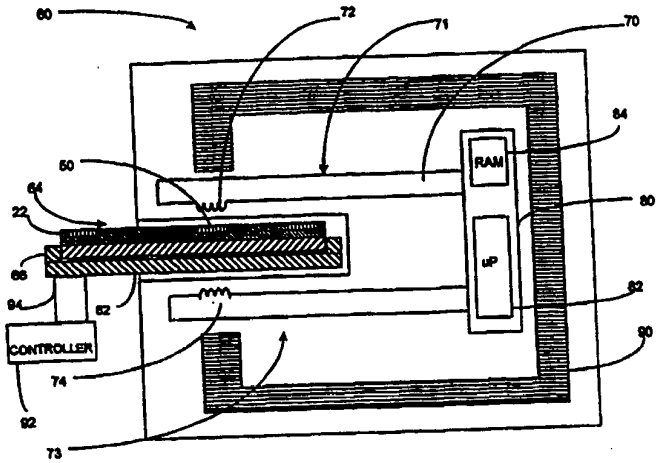

(57) Abstract

The integrated circuit die incorporates a test circuit portion that includes a first electromagnetic receiver for receiving wireless electromagnetic radiation, and a first electromagnetic transmitting element for transmitting wireless electromagnetic radiation in response to the electromagnetic radiation received by the first electromagnetic receiver. The test apparatus includes a second electromagnetic transmitter for transmitting wireless electromagnetic radiation to the first receiver of the integrated circuit die, and a second electromagnetic receiver for receiving wireless electromagnetic radiation transmitted by the first transmitter of the integrated circuit die. According to the method of testing the semiconductor integrated circuit die, test signals are transmitted wirelessly from the test device to the test circuit portion of the semiconductor integrated circuit die. In response to those transmitted test signals, the test circuit portion of the die performs a test sequence, and transmits wireless response signals.

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WIRELESS TEST APPARATUS FOR INTEGRATED CIRCUIT DIE

CROSS-REFERENCE TO RELATED APPLICATIONS

Not applicable.

FEDERALLY SPONSORED RESEARCH

Not applicable.

BACKGROUND OF THE INVENTION

The present invention relates to testing individual integrated circuit devices. In particular, the present invention relates to testing individual die or chips when they are in wafer form, in bare die form, or in packaged device form.

Integrated circuit die, and in particular semiconductor integrated circuit die, are manufactured by fabricating several individual die or chips on a wafer. After fabrication, the wafer is cut up, or diced, into the individual die.

Before the wafer is cut into the individual die, the manufacturer may desire to test the individual die on the wafer. After testing, those die that the test had determined to be defective are then marked. After the wafer is cut into individual die, the marked (defective) die are discarded. Such testing at the wafer stage permits the manufacturer to discard defective die prior to incurring the expense of packaging such defective die.

The manufacturer may also want to test the individual die after the wafer has been cut into the individual die, but before the die are packaged. Such testing identifies defective die, which are then discarded. Die testing permits the manufacturer to discard die the test determines are defective prior to incurring the expense of packaging such defective die.

Typically the individual die are tested at the wafer or bare die stages by contacting the die with test probes. A first test input probe contacts a test input contact pad fabricated on each die, activates the circuitry on the die, and executes a test of the chip by applying a particular test signal to the die. A second probe contacts another test contact pad on the die to detect how the circuitry of the die responds to the test. Die failing the test are discarded.

The manufacturer may also be interested in testing the device after it has been packaged. Input and output pins are provided on the packaged device to permit test signals to be applied to the device, and for the response signals to be read from the device. The packaged device may be placed in a test apparatus having receptacles or plug openings that correspond to the pins of the packaged device.

One issue that arises in such testing of die (whether at the wafer stage, at the bare die stage, or at the packaged device stage) is that contact pads must be included in the die design to provide points on the die for the test probes to contact or for the test pins of the packaged device. Depending on the circuit or function to be tested, it may be necessary to include one or more contact pads on the die for the sole purpose of testing the die. Such contact pads may serve no useful purpose after testing is completed. Yet those test contact pads continue to occupy space on the die. Such test contact pads may displace pads that could be used for other purposes. In addition, the space consumed by such test contact pads could be used to increase the space available on the die for functional die circuitry. Alternatively, the space used for test contact pads could be used to reduce the size of the die, which would permit more die to be manufactured or fabricated on a wafer.

An additional issue in designing a die for testability is that contact pads are typically placed around the perimeter of the die. However, the circuit to be tested may be in a central part of the die. A conductive path, or trace, must be provided from the circuit to be tested to the corresponding contact pad(s). Each such conductive trace in the circuitry on a die complicates the overall design of the die circuitry. If the need to connect internal test circuits to perimeter contact pads could be eliminated, the design of integrated circuits could be simplified.

A further issue is the significant risk of damaging the device in the testing process. Using test probes to contact the bare die (before packaging, in either wafer form, or in individual die form) carries the physical risk of damage from probe contact. Currently, to rapidly test multiple die, test probes are rapidly placed into contact with the test contact pads of the die. However, such rapid contact increases the risk that the probes will physically damage the die. When the device is tested in packaged form, inserting and removing the packaged device from the tester risks bending or breaking the pins on the packaged device. Therefore, die testers must balance the speed of testing die with the risk of physical damage.

SUMMARY OF THE INVENTION

The present invention is a system and method for testing semiconductor integrated circuit die, and a semiconductor integrated circuit die for testing by that system.

In accordance with the present invention, the circuitry of the die is probed electromagnetically to identify defects in the fabrication of the die. A test device includes a transmitter element to couple wirelessly one or more test patterns to a matching receiver in the die. An electromagnetic transmitter or radiator on the die transmits or radiates response signals from the die. The matching receiver in the test device receives the response signals. The transmitters and matching receivers may be inductors.

The integrated circuit die incorporates a test circuit portion. The test circuit portion includes an electromagnetic receiver for receiving wireless electromagnetic radiation. The die test circuit portion additionally includes an electromagnetic radiating element for emitting or transmitting wireless electromagnetic radiation in response to the electromagnetic radiation signals received by the die electromagnetic receiver. The test apparatus includes an electromagnetic transmitter for transmitting wireless electromagnetic radiation to the receiver of the integrated circuit die, and an electromagnetic receiver for receiving wireless electromagnetic radiation transmitted by the integrated circuit die.

In a preferred form, the test apparatus extends along opposite sides of the die to be tested, so that the strength and specificity of the coupling between the test apparatus and the die being tested is increased.

According to the method of testing the semiconductor integrated circuit die in accordance with the invention, wireless test signals are transmitted from a test device to a test circuit portion of the semiconductor integrated circuit die. In response to those transmitted test signals, the die performs a test sequence, and transmits wireless response signals. The test apparatus detects the response signals transmitted by the integrated circuit die.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a semiconductor wafer containing a plurality of individual die that may be tested in accordance with the present invention.

Figure 2 is a representation of a semiconductor integrated circuit die on the wafer shown in Figure 1.

Figure 3 is a cross-sectional view of the die of Figure 2, taken along the line 3-3 of Figure 2.

Figure 4 is a partial schematic diagram of a portion of the circuitry of the die of Figure 2.

Figure 5 is a diagram of the test apparatus incorporating an aspect of the present invention.

Figures 6a and 6b are schematic diagrams of oscillators that may be used in an embodiment of the present invention.

Figure 7 is a schematic diagram of a receiver that may be used in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Semiconductor integrated circuits are typically formed by fabricating a wafer containing several individual integrated circuits, or die. Typically, all the die on a single wafer are identical.

THE SEMICONDUCTOR DIE

A representative wafer 20 containing several individual die is shown in Figure 1. A particular individual die 22 is identified. The die 22 is designed and fabricated in accordance with an aspect of the present invention, as described below. Typically all the die on a wafer are identical. Therefore, all the other die on the wafer 20 may be considered to be identical to the die 22, so the die 22 will be described herein as representative of the die on the wafer. The wafer 20 may contain some partial die 24 at the edges of the wafer 20. Many techniques for fabricating such wafers are generally known and available in the semiconductor manufacturing arts.

After the wafer 20 is fabricated, the wafer is "diced" into the individual die, such as the die 22. The process of dicing semiconductor wafers into the individual die is well understood in the art. Lasers or mechanical saws are conventionally used to dice the wafer into its individual die. Each separate individual die 22 may then be packaged using any of the conventionally available packaging techniques.

The representative semiconductor integrated circuit die 22 incorporating an aspect of the present invention is shown in Figure 2 as it may appear before being packaged.

The die 22 includes a circuitry portion 30, which contains the operational circuitry of the die. Typically, the circuitry 30 occupies the central portion of the die 22. Contact pads 32 around the perimeter of the die 22 provide contact points between the circuitry 30 and other devices or elements. When the die 22 is packaged, the wires for the packaged device contact the contact pads 32 on the die. Conductive leads or traces 34 connect the appropriate portions of the circuitry 30 with the corresponding contact pads 32. These elements are common in the semiconductor integrated circuit industry, and are well understood.

The die 22 is substantially flat. The cross-sectional view of Figure 3 shows that the die 22 has a substrate layer 40, and a circuit layer 42. Consistent with conventional semiconductor integrated circuit technologies, the circuit elements are formed in the circuit layer 42 of the die 22. The die has a first, or upper, surface 46, and a second, or lower, surface 48. The upper and lower surfaces 46, 48 are substantially flat, and are substantially parallel with one another. This structure is also common and well known in the semiconductor integrated circuit arts.

In accordance with an aspect of the present invention, the circuitry 30 of the die 22 includes one or more test circuit portions 50 (Figure 2). The test circuit portion 50 may be placed wherever convenient on the die 22. Generally, the test circuit portion will be a portion of the die circuitry 30.

The test circuit portion 50 includes a test circuit 52 (shown representatively in Figure 4) that is to be tested, a receiver element 54, and a transmitter or emitter element 56. The test circuit portion receives wireless test signals at the receiver element 54. The test signals activate the test circuit 52, and cause the test circuit to perform one or more test sequences. In response to the test sequence(s), the test circuit produces test response signals to the emitter element 56. The emitter element 56 radiates or wirelessly transmits those response signals.

The test circuit 52 may be a regular part of the functioning die circuitry 30. or may be a special test circuit designed specifically for testing purposes. The details of the design of the test circuit depend on the specific function or attribute of the circuitry 30 that is to be tested. The test circuit 52 is designed to receive an input test signal. If

the test circuit 52 operates as designed, it produces a test output signal in response to the test input signal. If the test circuit does not produce the proper response signal, that is an indication that there is a defect in the integrated circuit device. The test circuitry may be designed consistently with current integrated circuit design techniques. Those familiar with the design of integrated circuit devices will be familiar with different types of test circuits that may be designed in integrated circuits.

In accordance with an aspect of the present invention, the test input signals for the test circuit 52 are received wirelessly at the receiver element 54. The receiver element 54 is electrically connected to the test circuit 52 so that the receiver element 54 receives wireless electromagnetic test signals and applies the received signals to the test circuit 52 as input test signals. The receiver element 54 in the illustrated embodiment is an inductor for receiving inductively coupled signals and conducting those received signals to the test circuit 52. Those skilled in the art will recognize that other types of receivers for wirelessly receiving signals may be used in the test circuit portion 50. For example, a capacitive element could be used to receive capacitively coupled signals. In addition, more elaborate receivers, such as a radio frequency (RF) receiver, or a coherent optical receiver may be used to wirelessly receive test signals for the test circuit 52.

The test circuit response signals generated by the test circuit 52 in response to the signals received at the receiver 54 are radiated or transmitted wirelessly from a radiator or transmitter element 56 connected to the test circuit 52. The transmitter element 56 may also be an inductor for inductively coupling signals from the test circuit 52. Those skilled in the art will recognize that other types of transmitters may be used for the radiating element 56 in the test circuit portion 50. For example, a capacitive element could be used to capacitively couple signals from the test circuit 52. In addition, more elaborate transmitters, such as a radio frequency (RF) transmitter, or a coherent optical transmitter may be used to radiate or emit response signal information from the test circuit 52.

THE TEST APPARATUS

The test apparatus constructed in accordance with an aspect of the present invention generates test signals and wirelessly transmits those test signals to the receiver element 54 of the test circuit portion 50 of the die 22. An exemplary test

apparatus 60 is shown in Figure 5. The test apparatus 60 includes a test controller 80, test circuitry 70, a transmitter element 72, and a receiver element 74.

The test controller 80 generates test signals for testing the test circuit 52. Those test signals are communicated over the test device circuitry 70 to the test device transmitter 72. The test device transmitter 72 is part of a first, or transmitting, segment 71 of the test system 60. The transmitter 72 wirelessly transmits those test signals as electromagnetic energy to the test circuit portion 50 of the die 22. As noted above, the test circuit portion 50 of the die 22 performs a test sequence in response to the test signal, and emits or transmits a response signal. The test response signal emitted by the test circuit portion is received in the test device by the test device receiver 74. The received response signal is communicated from the receiver 74 over the test device circuitry 70 to the test controller 80. The receiver 74 is part of the test device receiving segment 73 of the test system 60.

The test circuitry 70 connecting the test controller 80 with the test device transmitter 72 and test device receiver 74 may be shared between the transmitting segment 71 and receiving segment 73. Alternatively, the circuitry for the transmitting segment 71 may be separated from the circuitry for the receiving segment 73 of the test device.

The test apparatus 60 includes an opening 64 for receiving the semiconductor integrated circuit die 22 for testing. A receptacle 62 holds the die to be tested 22 in the opening 64. The receptacle 62 may be a tray that is shaped to receive the die to be tested. If the die is to be tested while in wafer form, the tray 62 is shaped to receive the wafer. If the die is to be tested as a bare die, after the wafer has been diced, the tray 62 is shaped to correspond with the die. If the die is to be tested in its packaged form, the tray 62 is shaped to receive the packaged device. The tray 62 shown in Figure 5 is shaped to receive a single bare die 22. The die 22 rests with its lower surface 48 (Figure 3) on the surface of the tray 62. The tray 62 may include a rim 66 around its perimeter to aid in proper placement of the die on the tray. The rim 66 also aids in holding the die in place on the tray.

The tray 62 is designed so that the die may easily be placed into and removed from the tray with a minimum of handling, and a minimum possibility of damage. Those familiar with the handling of semiconductor integrated circuits and wafers of

semiconductor integrated circuits will be familiar with several types of wafer and die handling techniques.

The tray 62 is movable relative to the opening 64 in the test apparatus 60. In particular, the tray 62 may be moved into and out of the opening. This allows the tray 62 to carry the die 22 into the opening 64 so that the test circuit portion 50 on the die 22 is in proximity with the test device transmitter 72 and the test device receiver 74. In addition, if there is more than one test circuit portion 50 on the die 22, the tray may be moved first to place one of those test circuit portions in proximity to the test device transmitter and receiver 72, 74, and then the tray may be moved so that another of those test circuit portions is in close proximity with the test device transmitter and receiver 72, 74. Furthermore, when the tray 62 holds a wafer 20 containing a plurality of individual die 22, the tray carrying the wafer may be moved so that the test apparatus may successively test each die on the wafer. The tray 62 carrying the wafer may be moved to successively bring each individual die 22 into proximity with the test device transmitter and receiver 72, 74, so that each die on the wafer may be excessively tested by the test device 60.

To provide movement of the tray 62 relative to the remainder of the test device 60, the tray 62 may be mounted on tracks (not shown). The tracks may be placed along the bottom of the opening 64, and rollers or wheels (not shown) may be mounted on the underside of the tray 62. The tray may also be mounted on an external arm 94 that moves the tray into or out of the opening 64. The arm 94 may provide the tray with lateral movement in two dimensions. That two dimensional movement may be beneficial when more than one test circuit portion 50 in a single die are to be tested, or if the tray carries a wafer of multiple individual die, each of which has one or more test circuit portions. Movement of the arm 94 may be controlled by a controller 92. The controller 92 may include one or more electric motors, gears, and other conventional components. Other types of movable mountings for the tray 62 will suggest themselves to those skilled in the art.

Preferably, the test device transmitter 72 and the test device receiver 74 are on opposite sides of the opening 64. In the embodiment illustrated in Figure 5, the test device transmitter 72 is near the upper side of the opening 64, and the test device receiver 74 is near the lower side of the opening 64. Ideally, for maximum signal

coupling (as will be apparent from the description below), the test device transmitter 72 is directly above the test device receiver 74.

The test device (including the tray 62) and the integrated circuit die 22 are designed to cooperate so that, during testing, the test circuit portion 50 is near the test device transmitter 72 and the test device receiver 74. In the illustrated embodiment, the tray 62 carries the die 22 into the opening 64 so that the test circuit portion 50 of the die is between the test device transmitter 72 and the test device receiver 74. This placement provides for the test device transmitter 72 to be in close proximity to the receiver element 54 (Figure 4) of the test circuit portion 50, and for the test device receiver 74 to be in close proximity to the emitter element 56 (Figure 4) of the test circuit portion 50.

With the test device transmitter 72 and the die receiver 54 in close proximity, the test device transmitter 72 may wirelessly couple signals to the die receiver 54 to activate the test circuit 52 and execute tests in the test circuit 52. Similarly, with the die emitter 56 and the test device receiver 74 in close proximity, the die emitter 56 may wirelessly couple signals such as test response signals to the test device receiver 74.

As will be recognized and understood by those skilled in the art, a moving electrical charge (a current) generates a magnetic field. A moving magnetic field generates an electric field having a voltage, which can give rise to an electrical current. This pair of phenomena allows the electrical signals or the electrical effects in the test device transmitter 72 to be wirelessly communicated to the receiver 54 of the test circuit portion 50 of the die 22.

For maximum coupling, the die 22 is positioned within the opening 64 so that the test circuit portion 50 on the die is less than ten centimeters from the test device transmitter 72, and also less than ten centimeters from the test device receiver 74. Preferably, the test circuit portion 50 is placed within three centimeters of the test device transmitter 72, and also within three centimeters of the test device receiver 74.

Test patterns may be radiated by the transmitter element 72 of the test fixture circuitry directly to the die receiver element 54 in the test circuit portion 50 of the integrated circuit die 22. Inductive coupling may be used for that purpose. In that case, the test device transmitter 72 is an inductor, and the receiver element 54 of the die test circuit portion 50 is also an inductor. Capacitive coupling between a capacitive

element as the test device transmitter 72 and a capacitive element as the receiver 54 of the die test circuit portion 50 may also be used.

For direct coupling of the test signals, such as by inductive coupling from the test device transmitter 72 to the test circuit portion 50 of the die under test 22, the illustrated arrangement in which the transmitter 72 and the receiver 74 are directly above and below the test circuit portion 50, respectively, provides the highest degree of electromagnetic coupling. A low reluctance flux return path 90 between a point near the test device transmitter 72 and test device receiver 74 improves the coupling from the test device and the specific test circuit portion of the die 22. So focusing the electromagnetic coupling reduces the likelihood that circuits on the die 22 other than the intended test circuit portion 50 are activated, and reduces the possibility of the test device receiver 74 detecting electromagnetic radiation emitted by other portions of the die 22. The low reluctance flux return path 90 may be a strand of wire, or a rigid frame within the test device 60. The exact configuration that works best and provides the most effective trade-off between cost and performance may be determined by those skilled in the art for each application.

Alternatively, the test patterns may be encoded onto electromagnetic radiation that is wirelessly transmitted by the test device transmitter 72. For example, the test device transmitter 72 may include a transmitting oscillator circuit for modulating the information onto a radio-frequency (RF) carrier. The test device transmitter 72 converts electrical signals on the test device circuitry 70 into electromagnetic radiation that corresponds to those signals. For example, the information of a first electrical signal generated by the test controller 80 may be modulated onto a radio frequency (RF) carrier wave generated by the transmitter 72. The receiver element 54 of the die test circuit portion 50, in close proximity to the test device transmitter 72, detects the emitted radiation. In the example in which the information is modulated onto a radio frequency carrier signal, the receiver 54 detects the radio frequency signal, and demodulates it to recover the information from the signal for use by the test circuit 52.

In one form, the transmitter 72 modulates or encodes the signal onto an RF carrier. The receiver 54 of the circuit portion 50 then demodulates or decodes the information from the RF signal. Such encoding or modulation allows the receiver 54 of the test circuit portion 50 to distinguish the RF signals emanating from the test device transmitter 72, and to distinguish those signals from the background noise.

Simple modulation and demodulation schemes may be used for modulating test patterns onto electromagnetic carrier signals, such as RF signals. Such modulation maximizes the likelihood of a strong signal coupling between the radiating element and the receiving element.

An NPN Hartley oscillator as shown in Figure 6a may be used for modulation purposes. Alternatively, an NPN Colpitts oscillator as shown in Figure 6b may be used. The Hartley and Colpitts oscillators, as well as other oscillators that may also be incorporated in the test device transmitter 72, are well understood in the art. The modulation may be amplitude modulation, frequency modulation, or spread spectrum encoding. The oscillators shown in Figures 6a and 6b are most useful for amplitude modulation. Frequency modulation and spread spectrum signals may require more sophisticated implementations. Useful instruction may be found in the *McGraw-Hill Encyclopedia of Science and Technology*, published by McGraw-Hill and Company, and in *The Radio Amateur's Handbook*, published by the American Radio Relay League. Those skilled in the art will also find information in *The Electrical Engineering Handbook*, (edited by R. C. Dorf, and published by the CRC Press), and in *Reference Data for Engineers: Radio, Electronics, Computer, and Communications*, (edited by E. C. Jordan and published by Howard W. Sams & Co.).

If the transmitter 72 transmits RF energy, the die receiver element 54 (Figure 4) is designed to receive and demodulate such RF signals. An exemplary receiver that may be used in the die test circuit portion 50 is shown in Figure 7.

Those skilled in the art will recognize that other methods of wirelessly transmitting information may be used in the transmitter 72. For example, infrared radiation may be used to carry the information. An infrared generator (not shown) in the transmitter 72 may be used to encode information onto an infrared beam. Yet further embodiments may incorporate one or more lasers (not shown) to transmit information. The information is modulated or encoded onto a beam of coherent optical radiation (light) emitted by the laser. In each of those embodiments, a corresponding receiver is incorporated in the die test circuit portion 50 as the receiver 54.

Those skilled in the art will recognize that the test patterns that may be transmitted by the test device transmitter 72 to test a particular test circuit 52 will vary depending on the nature of the test circuit 52. Those skilled in the design and testing of microelectronic circuits will be familiar with the different types of test signals that

may be useful in testing those circuits. The test patterns radiated by the test circuit radiating element 72 to the test circuit portion 50 of the integrated circuit die 22 are generated by the test controller 80. A variety of constructions are possible for the test controller 80. The test controller 80 may include, for example, a programmed microprocessor 82 and one or more Random Access Memory devices 84. Those skilled in the art will also recognize how those patterns may be generated by the test controller 80.

Predetermined sets of codes may be stored in the RAM 84. These codes are designed to test a specific circuit. They include a predetermined test sequence, and a predetermined response sequence. When the test sequence is applied to the circuit under test, the circuit produces the known response sequence if the circuit is operating properly. Therefore, the test controller 80 compares the response sequence received from the circuit portion 50 with the expected response sequence. If the received response sequence does not match the stored, expected response sequence bit for bit, or character for character (depending on the level of the test), the circuit portion 50 is presumed defective. The microprocessor 82 in the test controller 80 tracks which test is run, and whether a defect has been detected. The microprocessor 82 may also control the movement of the tray or receptacle 62 holding the die 22 by sending control signals to the controller 92 that directs the movement of the arm 94 holding the receptacle 62. Alternatively, the controller 92 may include a microprocessor or another element to provide direction to the arm 94.

The response signals generated by the die test circuit 52 and emitted by the die emitter element 56 of the test circuit portion 50 of the integrated circuit die 22 may also be radiated or transmitted directly to the test device receiver 74, or may be modulated onto an electromagnetic carrier signal for radiation or transmission to the receiver 74 of the test fixture.

For simplicity of design, it is preferred that the test circuit emitter 56 of the die test circuit portion 50 communicates to the test device receiver 74 in the same manner as a test device transmitter 72 communicates with the die test circuit receiver 54. For example, in the illustrated embodiment, inductive coupling is used to communicate test signals from the test device transmitter 74 to the receiver 54 of the test circuit portion 50 of the die 22. Inductive coupling is also used to transfer signals from the emitter element 56 of the test circuit portion 52 to the receiver 74 of the test device.

In an embodiment in which the response signals generated by the test circuit 52 are to be modulated onto a carrier for transmission to the test device receiver 74, an oscillator such as one of the oscillators shown in the circuit diagrams of Figures 6a and 6b may be used. In that circumstance, the test device receiver 74 may include a receiver section similar to that shown in Figure 7. Again, these elements are well understood by those familiar with a wireless transmission of information.

Those skilled in the art will recognize that a large number of options are possible for the transmission and reception segments of the test device 60. For example, in certain embodiments, the test circuit portion 50, and the inductors 72, 74 shown in Figure 5 may all be associated with coupling the test signal to the semiconductor die 22. A similar set of elements (not shown) may be included in the test device 60 to receive the response signal from the die 22. Those elements may be displaced from the elements 72, 74 so that the receiving elements of the test device do not directly receive the test signal from the transmitting elements 72, 74.

Alternatively, the transmitter 72 of the test device may modulate the test signals onto a first carrier frequency, and the transmitting section 54 (Figure 4) of the test circuit portion 50 may modulate the response signals onto a second carrier frequency.

In yet another implementation, the test device transmitter 72 and the transmitting section 56 (Figure 4) of the die test circuit portion 50 may modulate the test and response signals onto the same carrier frequency, but use mutually orthogonal modulation schemes. In this implementation, the test device transmitter 72 uses a first modulation scheme, and the transmitting section 56 (Figure 4) of the test circuit portion 50 on the die 22 uses a second modulation scheme, wherein the first and second modulation schemes are mutually orthogonal. With mutually orthogonal modulation schemes, the response receiver 74 of the test device does not "hear" the test device transmitter 72, and the receiving section 54 of the test circuit portion 50 does not "hear" the transmitting section 56.

Those skilled in the art will recognize that several individual test circuit portions such as the test per circuit portion 50 shown in Figure 2 may be included on a particular semiconductor integrated circuit die 22. Each such test circuit portion on the integrated circuit die is tested by a signal transmitted from a test device transmitter such as the transmitter 72. The response wirelessly radiated by each such test circuit portion is received by a corresponding test device receiver such as the test device

receiver 74. Each test circuit portion 50 on the die may be individually activated by using modulation schemes with different carrier frequencies for the different test circuit portions.

Those skilled in the art will also recognize that in lieu of separate radiating and receiving elements 72, 74 in the transmitter test circuit for each test circuit portion 50 on a die, a single pair of test device transmitting and receiving devices 72, 74 can be used to test multiple test circuit portions on the die 22, with the tray 62 moving the die 22 so that the different test circuit portions 50 are successively brought into proximity with the single pair of test device radiating and receiving elements 72, 74.

Having been provided with the above description, those having skill in the art will be able to design a variety of specific embodiments and implementations to the invention. For example, other forms of generating beams of electromagnetic energy may be developed. In addition, a variety of the implementations are possible for activating the circuitry on the particular die to which the electromagnetic energy is directed. Furthermore, various implementations for controlling the electromagnetic energy sources will be apparent to those skilled in the art. Therefore, the above description is intended to be exemplary, and not limiting.

CLAIMS

WE CLAIM:

1. A system for testing a semiconductor integrated circuit die, the system comprising:
   a first test system portion for wirelessly coupling electromagnetic energy to said integrated circuit die;
   a second test system portion for wirelessly coupling electromagnetic energy from said integrated circuit die.

2. The test system of Claim 1, wherein said first test system portion comprises a first inductor for inductively coupling electromagnetic energy from said first inductor to said integrated circuit die, and said second test system portion comprises a second inductor for inductively coupling electromagnetic energy from said integrated circuit die to said second inductor.

3. The test system of Claim 2, wherein the said system additionally comprises a low reluctance flux return path between a point near said first inductor and a point near said second inductor.

4. The test system of Claim 3, wherein said semiconductor integrated circuit die has first and second substantially parallel surfaces, and wherein:
   said first test system portion may be positioned substantially adjacent said first surface of said integrated circuit die; and
   said second test system portion may be positioned substantially adjacent said second surface of said integrated circuit die.

5. The test system of Claim 1, additionally comprising a test controller coupled to said first test system portion and to said second test system portion.

6. A system for testing a semiconductor integrated circuit die, the system comprising:

a receptacle for receiving a semiconductor integrated circuit die;

a test controller for generating test signals;

an electromagnetic energy radiation element connected to said test controller for wirelessly radiating, to a semiconductor integrated circuit die in said receptacle, electromagnetic energy corresponding to said test signals generated by said test controller; and

an electromagnetic energy receiving element for wirelessly receiving electromagnetic energy from a semiconductor integrated circuit die in said receptacle in response to said test signals.

7. The system of Claim 6, wherein:
said radiation element comprises a first inductor; and
said receiving element comprises a second inductor.

8. The system of Claim 7, wherein said first and second inductors are adjacent said receptacle.

9. The system of Claim 8, wherein said first inductor is adjacent a first side of said receptacle, and said second inductor is adjacent a second side of said receptacle.

10. The system of Claim 7, wherein said test system additionally includes a low reluctance flux return path between said first inductor and said second inductor.

11. The system of Claim 6, wherein said electromagnetic energy receiving element is connected to said test controller.

12. The system of Claim 6, wherein said receptacle for receiving said semiconductor integrated circuit die comprises a receptacle for receiving a wafer containing said semiconductor integrated circuit die.

13. The system of Claim 12, wherein said receptacle is movable relative to said radiation element and said receiving element.

14. The system of Claim 6, wherein said receptacle comprises a receptacle for receiving a bare semiconductor integrated circuit die.

15. The system of Claim 6, wherein said receptacle comprises a receptacle for receiving a packaged device incorporating said semiconductor integrated circuit die.

16. A combination comprising a semiconductor integrated circuit die and an apparatus for testing said integrated circuit die, the combination comprising:

a semiconductor integrated circuit die incorporating a test circuit portion, wherein said test circuit portion includes a first electromagnetic receiver for wirelessly receiving electromagnetic radiation, and said test circuit portion additionally includes a first electromagnetic transmitter for wirelessly transmitting electromagnetic radiation in response to electromagnetic radiation received by said electromagnetic receiver; and

a test fixture comprising:

a second electromagnetic transmitter for wirelessly transmitting electromagnetic radiation to said first electromagnetic receiver of said integrated circuit die; and

a second electromagnetic receiver for wirelessly receiving electromagnetic radiation from said first electromagnetic transmitter of said integrated circuit die.

17. The combination of Claim 16, additionally comprising a test controller connected to said second transmitter and to said second receiver.

18. An integrated circuit designed for wireless testability, said integrated circuit comprising:

an electromagnetic receiver for receiving wirelessly transmitted electromagnetic energy;

a test circuit for performing a test sequence on signals received at said receiver to generate response signals; and

an electromagnetic transmitter for wirelessly transmitting electromagnetic energy corresponding to said response signals.

19. The integrated circuit of Claim 18, wherein:
said receiver comprises a first inductor; and
said transmitter comprises a second inductor.

20. A method of testing a semiconductor integrated circuit die, the method comprising the steps of:
providing a die having a circuit that performs a test sequence in response to a test signal and that wirelessly transmits a response signal indicative of the test sequence;
wirelessly transmitting a test signal to said semiconductor integrated circuit die; and
detecting said response signal transmitted by said integrated circuit die.

21. The method of Claim 20, wherein:
said step of wirelessly transmitting a test signal to said semiconductor integrated circuit die comprises inductively coupling electromagnetic energy to said semiconductor integrated circuit die; and
said step of detecting said response signals comprises inductively coupling electromagnetic energy from said integrated circuit die.

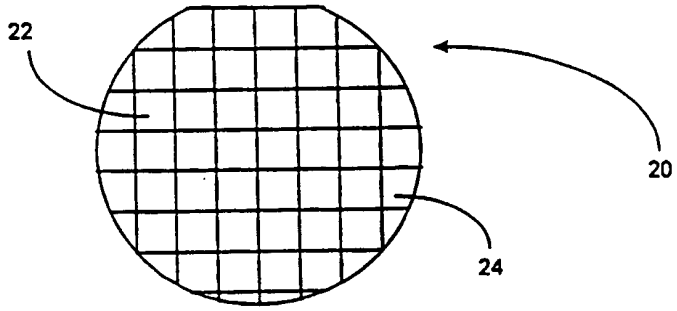

Figure 1

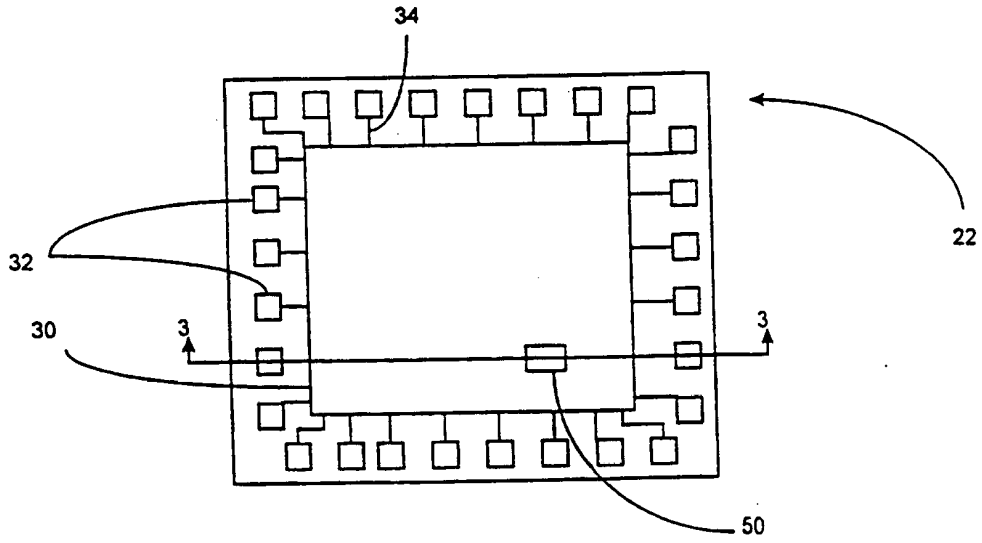

Figure 2

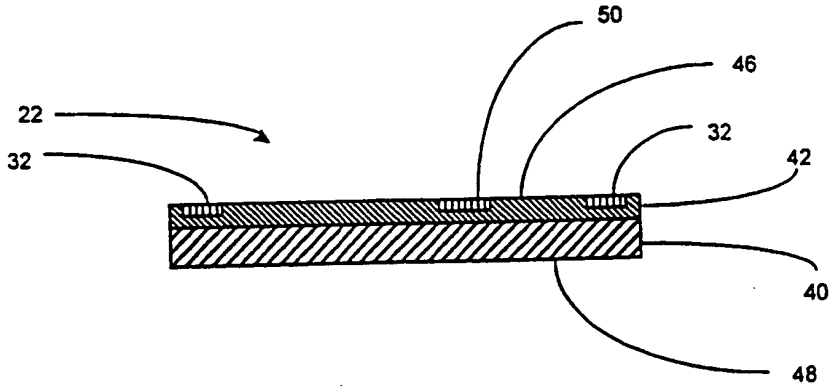

Figure 3

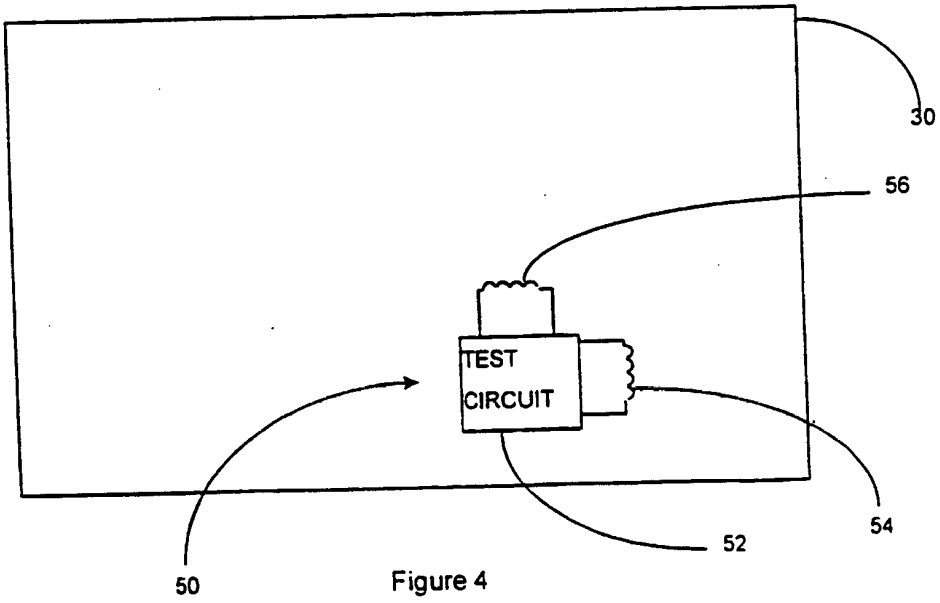

Figure 4

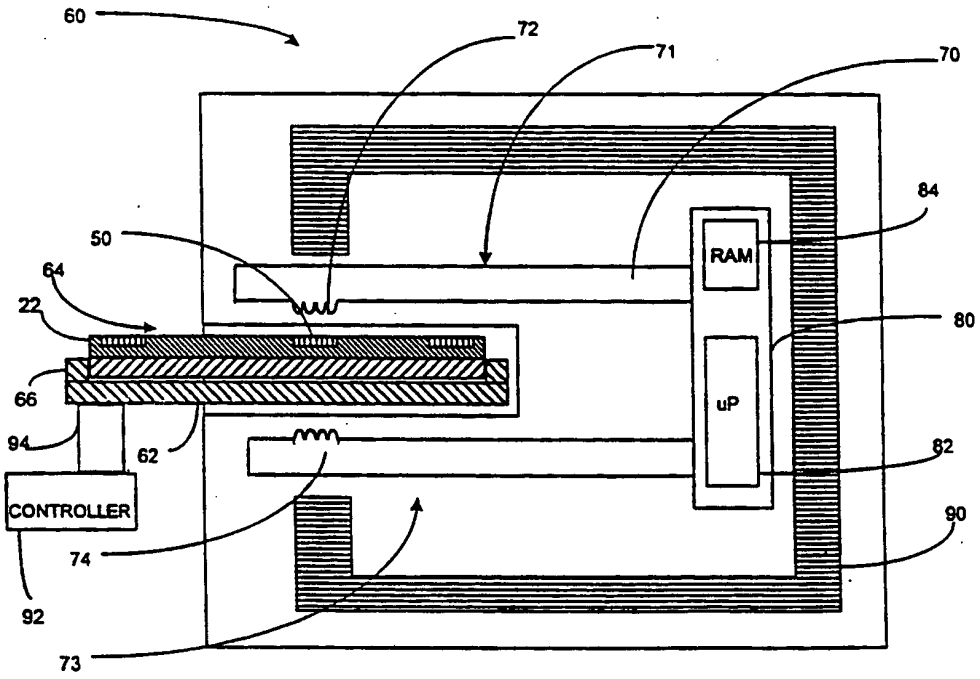

Figure 5

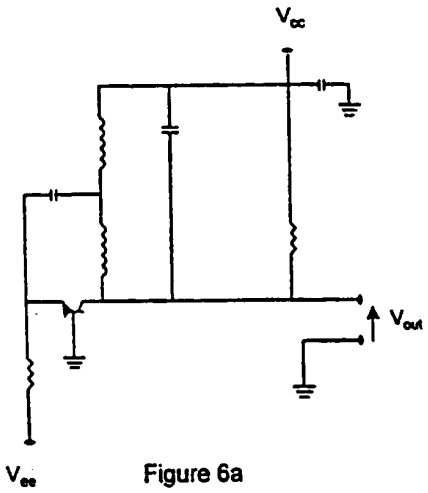

Figure 6a

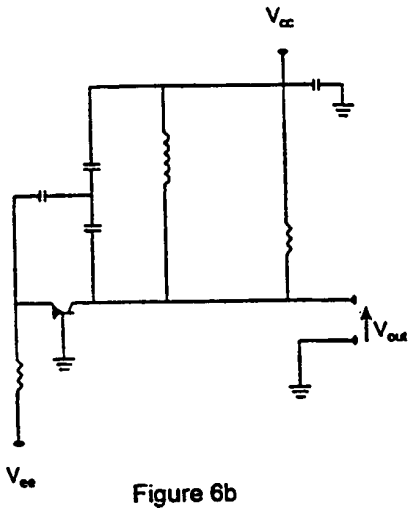

Figure 6b

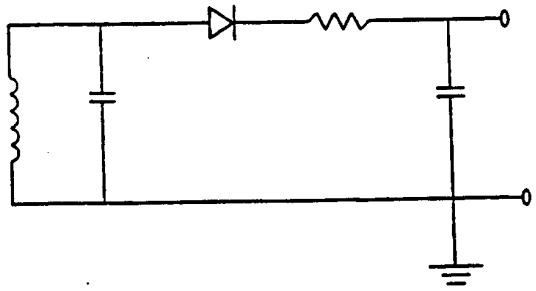

Figure 7

INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/US 98/27341

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G01R31/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 805 356 A (HEWLETTT-PACKARD COMP.) 5 November 1997 see column 3 - column 4; figure 5 ---	1,6, 16-21
A	DE 44 17 031 C (LANGER) 17 August 1995 see column 9, line 17 - line 20; figure 8.2 ---	1-21
A	DE 195 07 809 A (LANGER) 12 September 1996 see figure 2 -----	1-21

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 April 1999	19/04/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Hoornaert, W

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte ional Application No
PCT/US 98/27341

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 805356 A	05-11-1997	JP 10070160 A	10-03-1998
DE 4417031 C	17-08-1995	EP 0682264 A	15-11-1995
DE 19507809 A	12-09-1996	NONE	